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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	2

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,650	HOU ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 4, the phrase "etc." renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

3. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 5, the phrase "etc." renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 3, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al. (US 6,327,681 B1) in view of Bruce et al. (US 6,000,006).

As per claim 1, Yamagishi et al. teach a method of status display of DRAM which mainly through a monitor program to regularly detect the operation status of information integrity stored in various memory page of DRAM (figure 16c, abstract, col. 7, lines 6-11, lines 30-31, col. 13, lines 29-42, Yamagishi et al.) and display the tested result through display device (figure 1, col. 6, lines 35-37, Yamagishi et al.). However Yamagishi et al. do not explicitly teach the specific use of a method of defects recovery and, and to recover in real, wherein includes steps below:

a. Predetermine a spare memory page as temporary storage space for a tested page data;

b. Copy tested memory page data to pre-described spare memory page at the beginning of each test cycle;

c. Build a TLB to map the location of the tested memory page to the predetermined spare memory page, the tested memory page is relocated to predetermined spare memory page through TLB, which redirect follow up access operations to the spare memory page;

d. If there is no error occurs, back-store spare memory page data to the tested memory page, return the tested page to normal access operation and continue next memory page testing;

e. If there is any error occurs, monitor program will constantly block the said tested memory page, and any access operation to the said memory page will be redirected to the predetermined spare memory page according to TLB.

Bruce et al. in an analogous art teach that FIG. 1 is a prior-art replacement scheme for re-mapping defective pages of flash memory. Flash chip 10 has a memory array of EEPROM cells arranged into pages. Each page contains a 512-byte data field 12, and an additional 16-byte pointer field 14. Pointer field 14 contains a re-map bit (not shown) that is set when a defect is found in any of the 512 bytes of data in the page. When a page is read, the re-map bit is also read to determine if the page is defective. If defective, a pointer to another page is read from pointer field 14. The new page pointed to contains the replaced data.

For example, page 1 of FIG. 1 is defective. When page 1 at address 001 is read and found to be defective, pointer field 14 is also read. Pointer field 14 for page 1 contains the pointer 110. The address is changed to 110 so that the replacement page at address 110 is read to obtain the data for page 1.

Thus address 001 to page 1 is re-mapped by pointer field 14 to replacement page 6 at address 110. Page 6 was initially reserved as a spare page for later replacement of a defective page (figure 1, col. 1, lines 41-59, Bruce et al.).

Bruce et al. teach that FIG. 2 shows a prior-art re-mapping scheme using a bit-map table. To work around the problems of using the pointer fields in the flash memory pages, a separate re-map table in SRAM is used. SRAM re-map table 15 is accessed when the flash memory chip is accessed. Most logical addresses are simply passed through without translation or re-mapping since the corresponding bit in re-map table 15 is a zero. However, when a logical address's entry in re-map table 15 is a one, the logical address is re-mapped to a different physical address so that a replacement page is accessed (figure 2, col. 2, lines 1-11, Bruce et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamagishi et al.'s patent with the teachings of Bruce et al. by including an additional step of using a method of defects recovery and, and to recover in real, wherein includes steps below:

a. Predetermine a spare memory page as temporary storage space for a tested page data;

b. Copy tested memory page data to pre-described spare memory page at the beginning of each test cycle;

c. Build a TLB to map the location of the tested memory page to the predetermined spare memory page, the tested memory page is relocated to predetermined spare memory page through TLB, which redirect follow up access operations to the spare memory page;

d. If there is no error occurs, back-store spare memory page data to the tested memory page, return the tested page to normal access operation and continue next memory page testing;

e. If there is any error occurs, monitor program will constantly block the said tested memory page, and any access operation to the said memory page will be redirected to the predetermined spare memory page according to TLB.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity

to redirect the memory access to a defective memory location to another memory location and continue the system operation.

- As per claim 3, Yamagishi et al. and Bruce et al. teach the additional limitations.

Bruce et al. teach that the testing cycle is supplied by a counter (col. 3, lines 6-8, Bruce et al.). Yamagishi et al. teach the monitor program (col. 13, lines 41-42, Yamagishi et al.).

- As per claim 7, Yamagishi et al. and Bruce et al. teach the additional limitations.

Bruce et al. teach that during the step e, the tested memory page keeps in occupied state, until next memory page is tested, the monitor program will predetermine another spare memory page for tested memory page to keep on storing information, in the mean time, TLB will record memory page in which defects are discovered, and the corresponding relationship between next tested memory page and predetermined memory page (figure 1-2, col. 1, lines 41-59, col. 2, lines 1-11, Bruce et al.).

- As per claim 9, Yamagishi et al. and Bruce et al. teach the additional limitations.

Bruce et al. teach that the memory page inspection (col. 1, lines 47-48, Bruce et al.) further includes inspection method for which error correction code is included and if there is single bit error happened, it will be recorded that the memory page is unstable, and then recover it and strengthen the inspection (col. 9, lines 63-64, col. 10, lines 16-22, Bruce et al.); if single bit error happens again, then step e described in claim 1 will be executed to prevent single bit from transferring to binary error (col. 2, lines 8-11, Bruce et al.); if the error disappears, then step d described in claim 1 will be executed (col. 2, lines 5-8, Bruce et al.). Bruce et al. teach copying information to spare memory page (col. 1, lines 56-59, Bruce et al.). Yamagishi et al. teach the monitor program (col. 13, lines 41-42, Yamagishi et al.).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al. (US 6,327,681 B1) and Bruce et al. (US 6,000,006) as applied to claim 1 above, and further in view of Wilson (US 5,519,829).

As per claim 2, Yamagishi et al. and Bruce et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Yamagishi et al. and Bruce et al. do not explicitly teach the specific use of the monitor program that tests memory page is a page monitor program which inspects page by page.

Wilson in an analogous art teaches that FIG. 42 is a representation of the VRAM memory space, showing how pages of data are rendered in one section of the memory and then copied to another monitoring section of the memory (figure 42, col. 4, lines 25-28, Wilson). Wilson teaches that referring to FIG. 42, it is convenient that a predetermined section 830 of the VRAM 700 is always mapped to the monitor 40, and for simplicity the section will be considered between page addresses (0,0) and (7,7), (figure 42, col. 28, lines 17-20, Wilson).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamagishi et al.'s patent with the teachings of Wilson by including an additional step of using the monitor program that tests memory page is a page monitor program which inspects page by page.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to monitor a larger section of a memory and determine if it is defective.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al. (US 6,327,681 B1) and Bruce et al. (US 6,000,006) as applied to claim 1 above, and further in view of Tavallaei et al. (US 5,864,653).

As per claim 4, Yamagishi et al. and Bruce et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Yamagishi et al. and Bruce et al. do not explicitly teach the specific use of the display device liquid crystal device (LCD), monitor, etc.

Tavallaei et al. in an analogous art teach that the display 170 may include any console or monitor capable of receiving video data, such as a cathode ray tube (CRT), liquid crystal display (LCD), thin film transistor (TFT), or any other suitable computer display (col. 13, lines 64-67, col. 14, line 1, Tavallaei et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamagishi et al.'s patent with the teachings of Tavallaei et al. by including an additional step of using the display device liquid crystal device (LCD), monitor, etc.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the display device liquid crystal device (LCD), monitor, etc. would provide the opportunity to display the video data and provide monitored data to the tester.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al. (US 6,327,681 B1) and Bruce et al. (US 6,000,006) as applied to claim 1 above, and further in view of Jun (US 6,658,611 B1) and Lo et al. (US 4,922,451).

As per claim 5, Yamagishi et al. and Bruce et al. substantially teach the claimed invention described in claim 1 (as rejected above). Yamagishi et al. further teach displaying results including intact report, which enables users real time master the employment status of DRAM (figure 1, abstract, col. 6, lines 35-37, Yamagishi et al.). Bruce et al. further teach sum of memory usage (col. 4, lines 58-59, Bruce et al.). However Yamagishi et al. and Bruce et al. do not explicitly teach the specific use of testing frequency and detected fault.

Jun in an analogous art teaches that a specialized integrated circuit device tester is normally employed to perform manufacturing verification tests. For example, such an integrated circuit device tester may be used to perform read/write verification cycle tests on the memory array. Relatively low speed, low cost integrated circuit device testers are usually sufficient for detecting static defects in the memory array. However, extremely expensive integrated testers are needed to detect dynamic defects in very high-speed memory arrays. Unfortunately, such expensive high-speed integrated circuit testers increase the overall manufacturing costs for such devices. In addition, for integrated circuit devices that provide large memory arrays, the cycle time required to perform such read/write tests increases in proportion to the size of the array (col. 1, lines 21-35, Jun).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamagishi et al.'s patent with the teachings of Jun by including an additional step of using testing frequency and detected fault.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using testing frequency and

detected fault would provide the opportunity to determine the test cycle time needed to detect faults depending on the memory size.

Yamagishi et al. and Bruce et al. also do not explicitly teach the specific use of displaying actual memory size.

However Lo et al. in an analogous art teach that these routines, and other similar self test routines for checking the size of memory and any errors therein are well known and employed in most microcomputer systems (col. 4, lines 5-8, Lo et al.).

Lo et al. also teach that the remaining register 30 locations contain data resulting from the I/O memory size tests (figure 3, col. 4, lines 16-18, Lo et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamagishi et al.'s patent with the teachings of Lo et al. by including an additional step of displaying actual memory size.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that displaying actual memory size would provide the opportunity to determine the status of the memory and its effect on the system operation.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al. (US 6,327,681 B1) and Bruce et al. (US 6,000,006) as applied to claim 1 above, and further in view of Ge et al. (US 5,892,558).

As per claim 6, Yamagishi et al. and Bruce et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Yamagishi et al. and Bruce et al. do not explicitly teach specifically that the content displayed in display device is keeping unchanged until the beginning of next testing cycle.

Ge et al. in an analogous art teach that the data signals already applied to electrodes 26, 40 therefore will remain substantially unchanged so that the portions of the image displayed at such LC cells will remain intact until they are addressed in the next cycle (figure 1A, col. 5, lines 26-30, Ge et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamagishi et al.'s patent with the teachings of Ge et al. by including an additional step of displaying the content in display device that is keeping unchanged until the beginning of next testing cycle.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that displaying the content in display device that is keeping unchanged until the beginning of next testing cycle would provide the opportunity to analyze the content in the display device for each test cycle.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al. (US 6,327,681 B1) and Bruce et al. (US 6,000,006) as applied to claim 1 above, and further in view of Vaillancourt (US 5,299,202).

As per claim 8, Yamagishi et al. and Bruce et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Yamagishi et al. and Bruce et al. do not explicitly teach the specific use of a method, wherein the memory page inspection further includes inspection method for which error correction code (ECC) is not included, mainly through normal hardware test, which operates the continuous operation of write, then read to memory page, testing if the access is normal, if failed, it implies that there is error happened in the said memory page.

Vaillancourt in an analogous art teaches that once the allocation procedure (FIG. 10) has allocated a page, it runs a page test procedure (block 218), which is shown in more detail in FIG. 13, and tests the entire page of memory. Basically, the page test encompasses three separate tests: the page comparator test, the multiplexer/demultiplexer test, and the galloping write recovery test (col. 14, lines 11-17, Vaillancourt). Vaillancourt teaches that the read test of FIG. 14b reads data words that have been written in the immediately preceding pass of the write test of FIG. 14a. The value read from memory is compared with the data word written to memory and errors are noted (col. 15, lines 1-3, lines 8-10, Vaillancourt).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamagishi et al.'s patent with the teachings of Vaillancourt by including an additional step

of using a method, wherein the memory page inspection further includes inspection method for which error correction code (ECC) is not included, mainly through normal hardware test, which operates the continuous operation of write, then read to memory page, testing if the access is normal, if failed, it implies that there is error happened in the said memory page.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify if there is an error in the memory page and it will affect the system operation.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi

Patent Examiner

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